



PRELIMINARY

NLT Technologies, Ltd.

TFT COLOR LCD MODULE

NL204153AC21-17

54cm (21.3 Type)

QXGA

LVDS interface (4 ports)

PRELIMINARY DATA SHEET

DOD-PP-1266 (2nd edition)

**This PRELIMINARY DATA SHEET is updated
document from DOD-PP-1243(1).**

**All information is subject to change without notice.
Please confirm the sales representative before
starting to design your system.**

PRELIMINARY

NLT Technologies, Ltd.**NL204153AC21-17**

INTRODUCTION

The Copyright to this document belongs to NLT Technologies, Ltd. (hereinafter called "NLT"). No part of this document will be used, reproduced or copied without prior written consent of NLT.

NLT does and will not assume any liability for infringement of patents, copyrights or other intellectual property rights of any third party arising out of or in connection with application of the products described herein except for that directly attributable to mechanisms and workmanship thereof. No license, express or implied, is granted under any patent, copyright or other intellectual property right of NLT.

Some electronic parts/components would fail or malfunction at a certain rate. In spite of every effort to enhance reliability of products by NLT, the possibility of failures and malfunction might not be avoided entirely. To prevent the risks of damage to death, human bodily injury or other property arising out thereof or in connection therewith, each customer is required to take sufficient measures in its safety designs and plans including, but not limited to, redundant system, fire-containment and anti-failure.

The products are classified into three quality grades: "**Standard**", "**Special**", and "**Specific**" of the highest grade of a quality assurance program at the choice of a customer. Each quality grade is designed for applications described below. Any customer who intends to use a product for application other than that of Standard quality grade is required to contact an NLT sales representative in advance.

The **Standard** quality grade applies to the products developed, designed and manufactured in accordance with the NLT standard quality assurance program, which are designed for such application as any failure or malfunction of the products (sets) or parts/components incorporated therein a customer uses are, directly or indirectly, free of any damage to death, human bodily injury or other property, like general electronic devices.

Examples: Computers, office automation equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

The **Special** quality grade applies to the products developed, designed and manufactured in accordance with an NLT quality assurance program stricter than the standard one, which are designed for such application as any failure or malfunction of the products (sets) or parts/components incorporated therein a customer uses might directly cause any damage to death, human bodily injury or other property, or such application under more severe condition than that defined in the Standard quality grade without such direct damage.

Examples: Control systems for transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, medical equipment not specifically designed for life support, safety equipment, etc.

The **Specific** quality grade applies to the products developed, designed and manufactured in accordance with the standards or quality assurance program designated by a customer who requires an extremely higher level of reliability and quality for such products.

Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.



PRELIMINARY

NLT Technologies, Ltd.**NL204153AC21-17**

CONTENTS

INTRODUCTION	2
1. OUTLINE	4
1.1 STRUCTURE AND PRINCIPLE.....	4
1.2 APPLICATION	4
1.3 FEATURES.....	4
2. GENERAL SPECIFICATIONS	5
3. BLOCK DIAGRAM	6
4. DETAILED SPECIFICATIONS	7
4.1 MECHANICAL SPECIFICATIONS.....	7
4.2 ABSOLUTE MAXIMUM RATINGS	7
4.3 ELECTRICAL CHARACTERISTICS	8
4.3.1 LCD panel signal processing board	8
4.3.2 LED Driver board	9
4.3.3 LED Driver board current wave	9
4.3.4 Power supply voltage ripple.....	10
4.3.5 Fuse.....	10
4.4 POWER SUPPLY VOLTAGE SEQUENCE	11
4.4.1 LCD panel signal processing board	11
4.4.2 LED driver board	11
4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS.....	12
4.5.1 LCD panel signal processing board	12
4.5.2 LED driver board.....	15
4.5.3 Positions of socket	16
4.6 LUMINANCE CONTROL.....	17
4.6.1 Luminance control methods.....	17
4.6.2 Detail of BRTP timing	18
4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER.....	19
4.8 DISPLAY COLORS AND INPUT DATA SIGNALS	21
4.9 INPUT SIGNAL TIMINGS.....	22
4.9.1 Timing characteristics	22
4.9.2 Input signal timing chart	22
4.10 LVDS DATA TRANSMISSION METHOD	23
4.11 DISPLAY POSITIONS.....	23
4.12 PIXEL ARRANGMENT	24
4.13 OPTICS.....	25
4.13.1 Optical characteristics.....	25
4.13.2 Definition of contrast ratio.....	26
4.13.3 Definition of luminance uniformity	26
4.13.4 Definition of color uniformity	26
4.13.5 Definition of response times	27
4.13.6 Definition of viewing angles.....	27
5. ESTIMATED LUMINANCE LIFETIME	27
6. RELIABILITY TESTS	28
7. PRECAUTIONS	29
7.1 MEANING OF CAUTION SIGNS	29
7.2 CAUTIONS	29
7.3 ATTENTIONS	29
7.3.1 Handling of the product	29
7.3.2 Environment.....	30
7.3.3 Characteristics.....	31
7.3.4 Others.....	31
8. OUTLINE DRAWINGS	32
8.1 FRONT VIEW	32
8.2 REAR VIEW	33
REVISION HISTORY	34

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL204153AC21-17 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Color monitor system

1.3 FEATURES

- Ultra-wide viewing angle (Adoption of Ultra-Advanced Super Fine TFT (UA-SFT))
- Wide color gamut
- High luminance
- High contrast
- Low reflection
- 1,024 gray scale in each R, G, B sub-pixel (10-bit), 1,073,741,824 colors
- LVDS interface
- Selectable LVDS data input map
- Small foot print
- Long life LED backlight type with an LED driver board



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

2. GENERAL SPECIFICATIONS

Display area	433.152 (H) × 324.864 (V) mm
Diagonal size of display	54cm (21.3 inches)
Drive system	a-Si TFT active matrix
Display color	1,073,741,824 colors
Pixel	2,048 (H) × 1,536 (V) pixels (1 pixel consists of 3 sub-pixels (RGB).)
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Sub-pixel pitch	0.0705 (H) × 0.2115 (V) mm
Pixel pitch	0.2115 (H) × 0.2115 (V) mm
Module size	457.0 (W) × 350.0 (H) × 21.5 (D) mm (typ.)
Weight	(2,700)g (typ.)
Contrast ratio	1,400:1 (typ.)
Viewing angle	At the contrast ratio ≥ 10:1 • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale ($\gamma \approx$ DICOM): normal axis (perpendicular) Note1
Polarizer surface	Antiglare
Polarizer pencil-hardness	2H (min.) [by JIS K5600]
Color gamut	At LCD panel center (72) % (typ.) [against NTSC color space]
Response time	$T_{on} + T_{off}$ (10% ← → 90%) (40)ms (typ.)
Luminance	At the maximum luminance control 800cd/m ² (typ.)
Signal system	4 ports LVDS interface (THC63LVD104S×2pcs, THine Electronics, Inc. or equivalent) [RGB 10-bit signals, Data enable signal (DE), Dot clock (CK)]
Power supply voltage	LCD panel signal processing board: 12.0V LED driver board: 12.0V
Backlight	LED backlight type with LED driver board
Power consumption	At checkered flag pattern, the maximum luminance control (58)W (typ.)

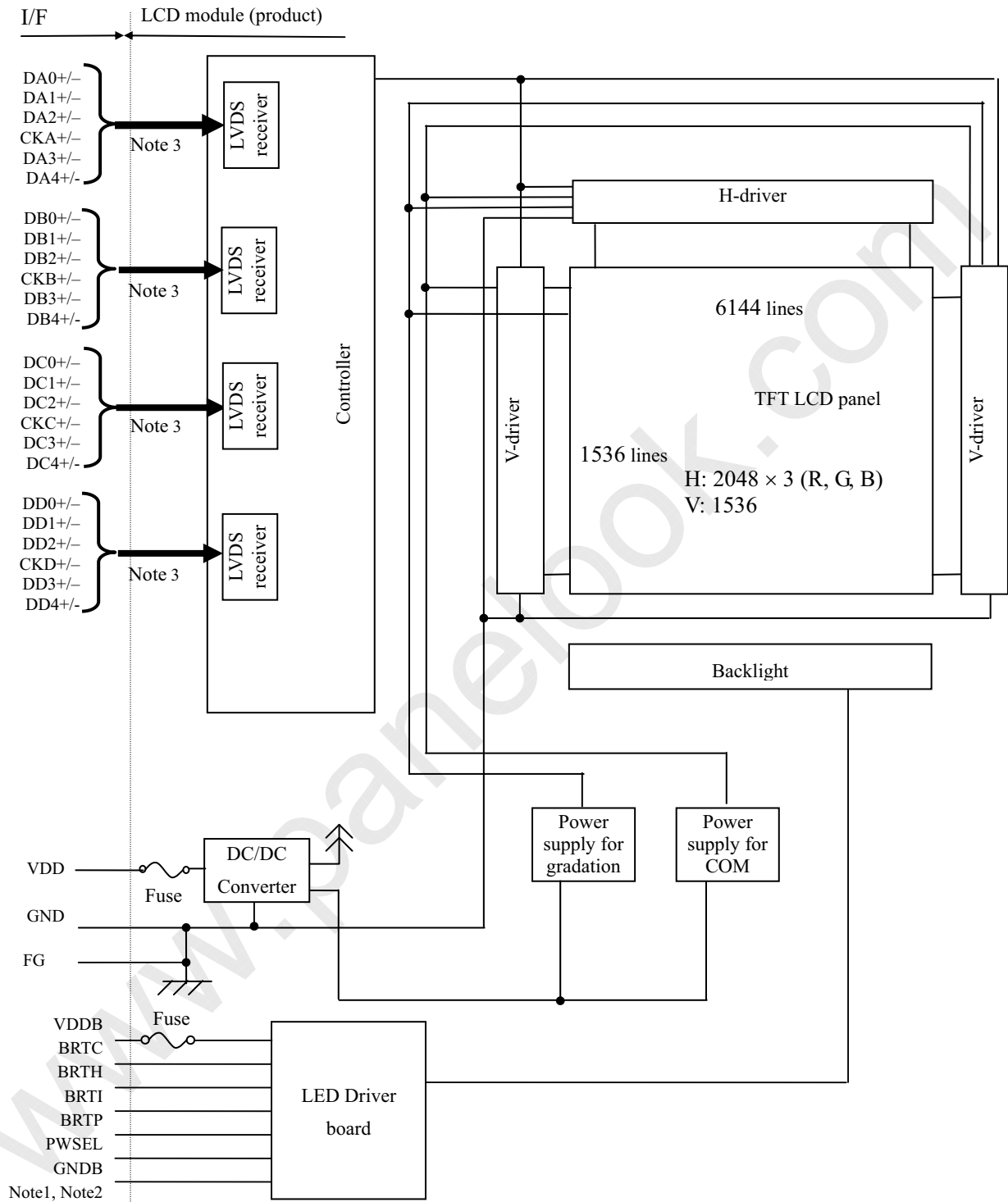
Note1: When the product luminance is 450cd/m², the gamma characteristic is designed to $\gamma \approx$ DICOM.

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (LED driver board ground) in the LCD module are as follows.

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2 GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds be connected together in customer equipment.

Note3 Each pair of the LVDS signal has a 100Ω terminating resistance between D+ and D-.



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ±1.0 (W) × 350.0 ±1.0 (H) × 21.5 (typ., D) 23.0 (max. D) Note1, Note2	mm
Display area	433.152 (H) × 324.864 (V) Note2	mm
Weight	(2,700) (typ.), (2,980) (max.)	g

Note1: Excluding warpage of the cover for LED driver board.

Note2: See "8. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	-
	LED driver board		VDDB	-0.3 to +15.0	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +2.8	V	VDD= 12.0V
	LED driver board	BRTI signal	VBI	-0.3 to +1.5	V	VDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature		Front surface	TopF	(0 to +60)	°C	Note2
		Rear surface	TopR	(0 to + 60)	°C	Note3
Relative humidity Note4			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
				≤ 70	%	50°C < Ta ≤ 55°C
Absolute humidity Note4			AH	≤ 73 Note5	g/m ³	Ta > 55°C
Operating altitude			-	≤ 4,850	m	0°C≤ Ta ≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C≤ Ta ≤ 60°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-, BSEL.

Note2: Measured at LCD panel surface (including self-heat)

Note3: Measured at LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta= 55°C and RH= 70%



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	(590) Note1	(980) Note2	mA	at VDD= 12.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-

Note1: Checkered flag pattern (by EIAJ ED-2522)

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS driver

Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

PRELIMINARY

NLT Technologies, Ltd.

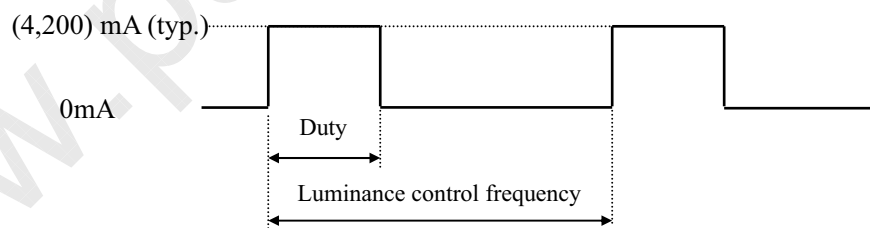
NL204153AC21-17

4.3.2 LED Driver board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDDDB	(11.4)	12.0	(12.6)	V	-
Power supply current		IDDB	-	(4,200)	TBD	mA	VDDDB= 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V
	BRTP signal	High	VBPH	2.0	-	5.25	V
		Low	VBPL	0	-	0.8	V
	BRTC signal	High	VBCH	2.0	-	5.25	V
		Low	VBCL	0	-	0.8	V
	PWSEL signal	High	VBSH	2.0	-	5.25	V
		Low	VBSL	0	-	0.8	V
							-
Input current for signals	BRTI signal		IBI	TBD	-	TBD	μA
	BRTP signal	High	IBPH	-	-	TBD	μA
		Low	IBPL	TBD	-	-	μA
	BRTC signal	High	IBCH	-	-	TBD	μA
		Low	IBCL	TBD	-	-	μA
	PWSEL signal	High	IPSH	-	-	TBD	μA
		Low	IPSL	TBD	-	-	μA
							-

4.3.3 LED Driver board current wave



At the maximum luminance control: 100%

At the minimum luminance control: (1)% (At frequency: 325 Hz)

Luminance control frequency: (255)Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "4.6.2 Detail of BRTP timing".

Note2: The power supply lines (VDDDB and GNDB) have large ripple voltage during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.3.4 Power supply voltage ripple

2

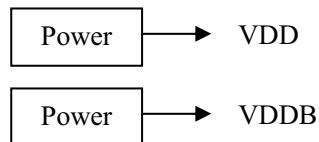
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Unit
VDD	12.0V	≤ 100	mVp-p
VDDDB	12.0V	≤ 200	mVp-p

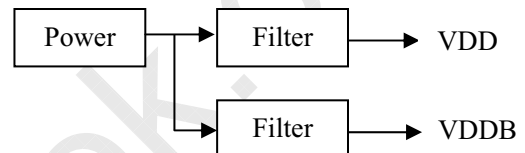
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



4.3.5 Fuse

2

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16202AB	KAMAYA ELECTRIC Co., Ltd.	2.0A	4.0A, 5 seconds maximum	Note1
			32V		
VDDDB	CCF1N10	KOA Corporation	10A	20 A, 1 seconds maximum	
			60 V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

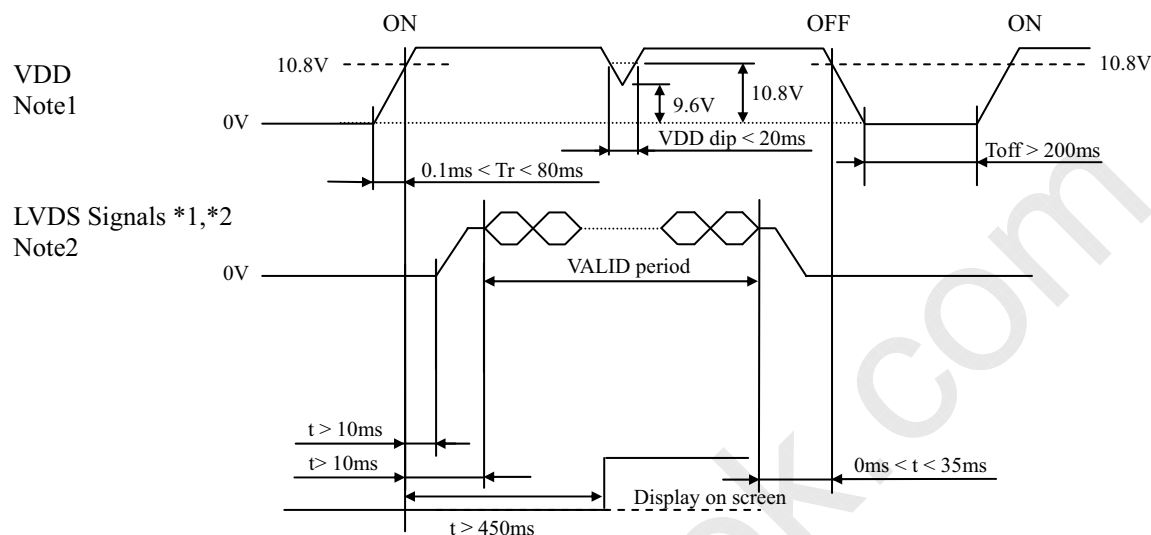
PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

*2: LVDS signals should be measured at the terminal of 100 Ω resistance.

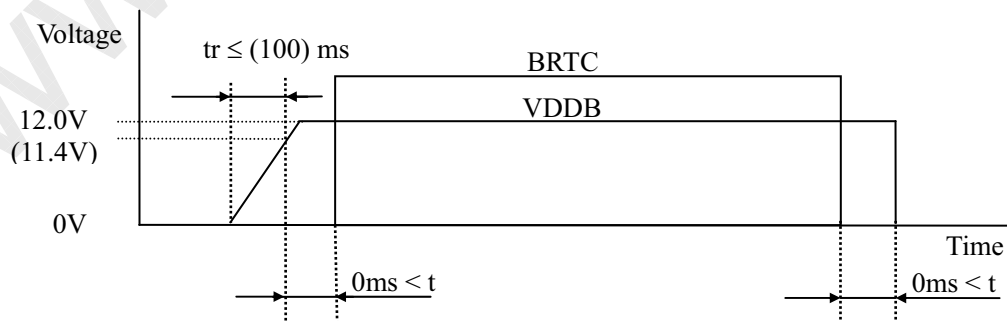
Note1: If there is a voltage variation (voltage drop) at the rising edge of VCC below 10.8V, there is a possibility that a product does not work due to a protection circuit.

Note2: LVDS signals must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage.

If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VCC also must be shut down.

Note3: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

4.4.2 LED driver board



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If t_r is more than (100) ms, the backlight will be turned off by a protection circuit for LED driver board.

Note3: When VDDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-RE51S-HF (Japan Aviation Electronics Industry Limited (JAE))

Adaptable plug: FI-RE51HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DA0-	Pixel data A0	LVDS differential data input Note2
5	DA0+		
6	GND	Ground	Note1
7	DA1-	Pixel data A1	LVDS differential data input Note2
8	DA1+		
9	GND	Ground	Note1
10	DA2-	Pixel data A2	LVDS differential data input Note2
11	DA2+		
12	GND	Ground	Note1
13	CKA-	Pixel clock A	LVDS differential data input Note2
14	CKA+		
15	GND	Ground	Note1
16	DA3-	Pixel data A3	LVDS differential data input Note2
17	DA3+		
18	GND	Ground	Note1
19	DA4-	Pixel data A4	LVDS differential data input Note2
20	DA4+		
21	GND	Ground	Note1
22	DB0-	Pixel data B0	LVDS differential data input Note2
23	DB0+		
24	GND	Ground	Note1
25	DB1-	Pixel data B1	LVDS differential data input Note2
26	DB1+		
27	GND	Ground	Note1
28	DB2-	Pixel data B2	LVDS differential data input Note2
29	DB2+		
30	GND	Ground	Note1
31	CKB-	Pixel clock B	LVDS differential data input Note2
32	CKB+		
33	GND	Ground	Note1
34	DB3-	Pixel data B3	LVDS differential data input Note2
35	DB3+		
36	GND	Ground	Note1
37	DB4-	Pixel data B4	LVDS differential data input Note2
38	DB4+		
39	GND	Ground	Note1



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

Continued

40	GND	Ground	Note1
41	RSEV	-	Keep this pin Open.
42	RSEV	-	Keep this pin Open.
43	RSEV	-	Keep this pin Open.
44	RSEV	-	Keep this pin Open.
45	GND	Ground	Note1
46	GND	Ground	Note1
47	GND	Ground	Note1
48	RSEV	-	Keep this pin Open.
49	RSEV	-	Keep this pin Open.
50	RSEV	-	Keep this pin Open.
51	GND	Ground	Note1

Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

CN2 socket (LCD module side): FI-RE41S-HF (Japan Aviation Electronics Industry Limited (JAE))

Adaptable plug: FI-RE41HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DC0-	Pixel data C0	LVDS differential data input Note2
5	DC0+		
6	GND	Ground	Note1
7	DC1-	Pixel data C1	LVDS differential data input Note2
8	DC1+		
9	GND	Ground	Note1
10	DC2-	Pixel data C2	LVDS differential data input Note2
11	DC2+		
12	GND	Ground	Note1
13	CKC-	Pixel clock C	LVDS differential data input Note2
14	CKC+		
15	GND	Ground	Note1
16	DC3-	Pixel data C3	LVDS differential data input Note2
17	DC3+		
18	GND	Ground	Note1
19	DC4-	Pixel data C4	LVDS differential data input Note2
20	DC4+		
21	GND	Ground	Note1
22	DD0-	Pixel data D0	LVDS differential data input Note2
23	DD0+		
24	GND	Ground	Note1
25	DD1-	Pixel data D1	LVDS differential data input Note2
26	DD1+		
27	GND	Ground	Note1
28	DD2-	Pixel data D2	LVDS differential data input Note2
29	DD2+		
30	GND	Ground	Note1
31	CKD-	Pixel clock D	LVDS differential data input Note2
32	CKD+		
33	GND	Ground	Note1
34	DD3-	Pixel data D3	LVDS differential data input Note2
35	DD3+		
36	GND	Ground	Note1
37	DD4-	Pixel data D4	LVDS differential data input Note2
38	DD4+		
39	GND	Ground	Note1
40	GND	Ground	Note1
41	GND	Ground	Note1

Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

CN3 socket (LCD module side): IL-Z-12PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))

Adaptable plug: IL-Z-12S-S125C (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	Note1
2	VDD		
3	VDD		
4	VDD		
5	VDD		
6	VDD		
7	GND	Signal ground	Note1
8	GND		
9	GND		
10	GND		
11	GND		
12	GND		

Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.2 LED driver board

CN201 socket (LCD module side): DF3Z-10P-2H (2*) (HIROSE ELECTRIC Co.,Ltd.)

Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co.,Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))

Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	Note2
6	BRTI		
7	BRTP	BRTP signal	Note1
8	GNDB	LED driver board ground	
9	PWSEL	Selection of luminance control signal method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.

Note2: See "4.6.1 LUMINANCE CONTROL".

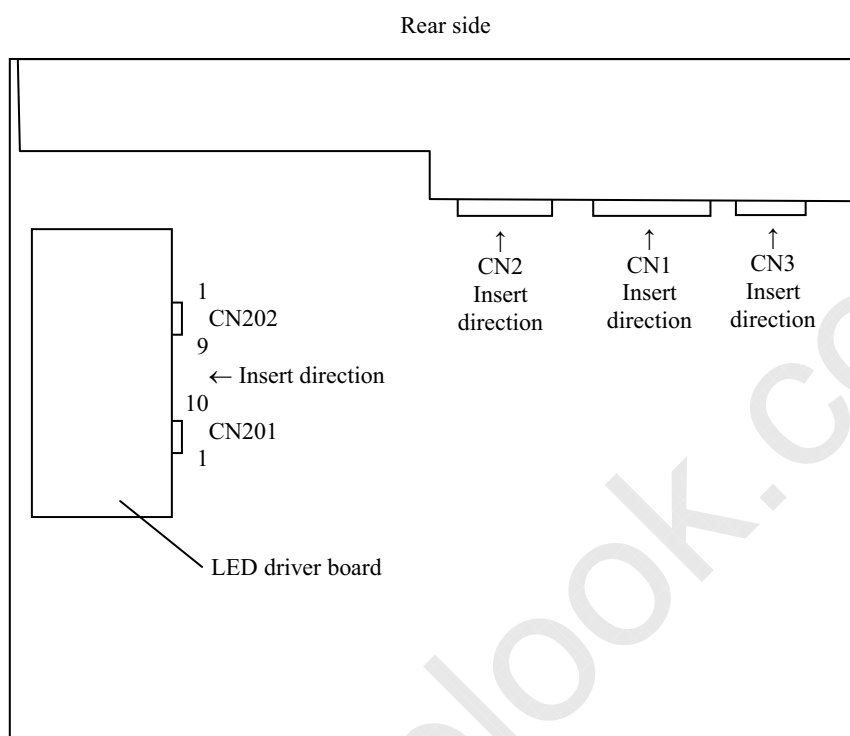
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.5.3 Positions of socket



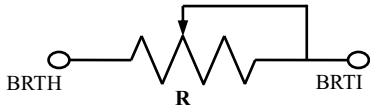
PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

Method	Adjustment and luminance ratio	PWSEL terminal	BRTP terminal						
Variable resistor control Note1	• Adjustment The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance. The resistor (R) must be connected between BRTH-BRTI terminals.  • Luminance ratio Note3 <table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>0Ω</td><td>0%(Min. Luminance)</td></tr><tr><td>10 kΩ</td><td>100% (Max. Luminance)</td></tr></table>	Resistance	Luminance ratio	0Ω	0%(Min. Luminance)	10 kΩ	100% (Max. Luminance)	High or Open	Open
Resistance	Luminance ratio								
0Ω	0%(Min. Luminance)								
10 kΩ	100% (Max. Luminance)								
Voltage control Note1	• Adjustment Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance. Luminance is the maximum when BRTI terminal is Open. • Luminance ratio Note3 <table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0V</td><td>0% (Min. Luminance)</td></tr><tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr></table>	BRTI Voltage (VBI)	Luminance ratio	0V	0% (Min. Luminance)	1.0V	100% (Max. Luminance)		
BRTI Voltage (VBI)	Luminance ratio								
0V	0% (Min. Luminance)								
1.0V	100% (Max. Luminance)								
Pulse width modulation Note1 Note2 Note4	• Adjustment Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal. • Luminance ratio Note3 <table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>(0.01)</td><td>(1)% (Min. Luminance) (At frequency: 325 Hz)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table>	Duty ratio	Luminance ratio	(0.01)	(1)% (Min. Luminance) (At frequency: 325 Hz)	1.0	100% (Max. Luminance)	Low	BRTP signal
Duty ratio	Luminance ratio								
(0.01)	(1)% (Min. Luminance) (At frequency: 325 Hz)								
1.0	100% (Max. Luminance)								

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

Use PWM method, if interference noises appear on the display image!

Note2: The LED driver board will stop working, if the Low period of BRTP signal is more than 50ms while BRTP signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver board will start to work when power is supplied again.

Note3: These data are the target values.

Note4: See "4.6.2 Detail of BRTP timing".

PRELIMINARY

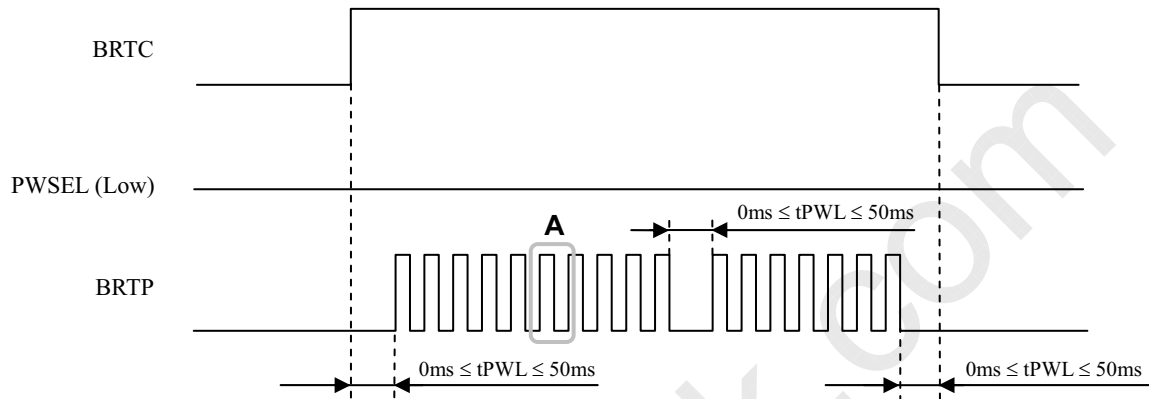
NLT Technologies, Ltd.

NL204153AC21-17

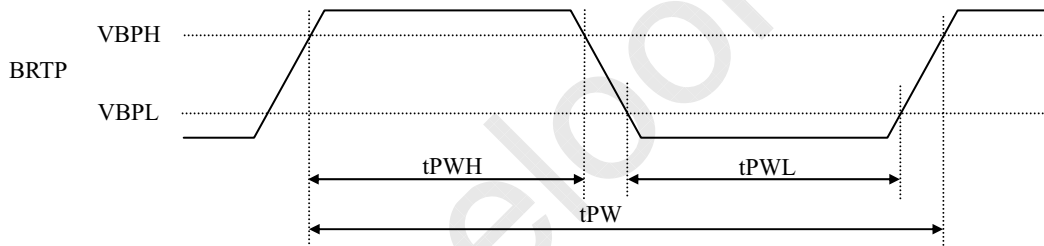
4.6.2 Detail of B RTP timing

(1) Timing diagrams

• Outline chart



• Detail of A part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	(185)	-	(1,000)	Hz	Note1, Note2
External PWM pulse width	tPWH	(30)	-	-	μs	Note1, Note3

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{tPW}, \quad DL = \frac{tPWH}{tPW}$$

Note2: See the following formula for luminance control frequency.

$$\text{Luminance control frequency} = 1/tv \times (n+0.25) \text{ [or } (n+0.75)]$$

$$n = 1, 2, 3 \dots$$

tv: Vertical cycle (See "4.9.1 Timing characteristics".)

The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!

Note3: See "4.6.1 Luminance control methods".



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER

	Bit mapping	Transmitter Pin Assign		Output Connector		CN1	
		Single type LVDS Tx	Dual type LVDS Tx Thine THC63LVD1023B			Pin No.	Signal Name
odd Pixel data A	RA4	TA0	R14	ATA-	→	-	-
	RA5	TA1	R15			4	DA0-
	RA6	TA2	R16			5	DA0+
	RA7	TA3	R17			-	-
	RA8	TA4	R18	ATB-	→	7	DA1-
	RA9	TA5	R19			8	DA1+
	GA4	TA6	G14			-	-
	GA5	TB0	G15			10	DA2-
	GA6	TB1	G16	ATC-	→	11	DA2+
	GA7	TB2	G17			-	-
	GA8	TB3	G18			16	DA3-
	GA9	TB4	G19			17	DA3+
	BA4	TB5	B14	ATD-	→	-	-
	BA5	TB6	B15			19	DA4-
	BA6	TC0	B16			20	DA4+
	BA7	TC1	B17			-	-
	BA8	TC2	B18	ATE-	→	13	CKA-
	BA9	TC3	B19			14	CKA+
	Hsync	TC4	Hsync			-	-
	Vsync	TC5	Vsync			22	DB0-
	DE	TC6	DE	ATD+	→	23	DB0+
	RA2	TD0	R12			-	-
	RA3	TD1	R13			25	DB1-
	GA2	TD2	G12	ATE+	→	26	DB1+
	GA3	TD3	G13			-	-
	BA2	TD4	B12			28	DB2-
	BA3	TD5	B13			29	DB2+
	N.C.	TD6	-	BTB-	→	-	-
	RA0	TE0	R10			34	DB3-
	RA1	TE1	R11			35	DB3+
	GA0	TE2	G10			-	-
	GA1	TE3	G11	BTC-	→	37	DB4-
	BA0	TE4	B10			38	DB4+
	BA1	TE5	B11			-	-
	N.C.	TE6	-			31	CKB-
even Pixel data B	CLK	CLK	CLK	ATCLK- ATCLK+	→	32	CKB+
	RB4	TA0	R14	BTA-	→	-	-
	RB5	TA1	R15			22	DB0-
	RB6	TA2	R16			23	DB0+
	RB7	TA3	R17	BTA+	→	-	-
	RB8	TA4	R18			25	DB1-
	RB9	TA5	R19			26	DB1+
	GB4	TA6	G14			-	-
	GB5	TB0	G15	BTB-	→	28	DB2-
	GB6	TB1	G16			29	DB2+
	GB7	TB2	G17			-	-
	GB8	TB3	G18	BTB+	→	34	DB3-
	GB9	TB4	G19			35	DB3+
	BB4	TB5	B14			-	-
	BB5	TB6	B15	BTC-	→	37	DB4-
	BB6	TC0	B16			38	DB4+
	BB7	TC1	B17			-	-
	BB8	TC2	B18	BTC+	→	31	CKB-
	BB9	TC3	B19			32	CKB+
	Hsync	TC4	Hsync			-	-
	Vsync	TC5	Vsync	BTD-	→	22	DB0-
	DE	TC6	DE			23	DB0+
	RB2	TD0	R12			-	-
	RB3	TD1	R13	BTD+	→	25	DB1-
	GB2	TD2	G12			26	DB1+
	GB3	TD3	G13			-	-
	BB2	TD4	B12	BTE-	→	28	DB2-
	BB3	TD5	B13			29	DB2+
	N.C.	TD6	-			-	-
	RB0	TE0	R10			34	DB3-
	RB1	TE1	R11	BTE+	→	35	DB3+
	GB0	TE2	G10			-	-
	GB1	TE3	G11			37	DB4-
	BB0	TE4	B10	BTCLK- BTCLK+	→	38	DB4+
	BB1	TE5	B11			-	-
	N.C.	TE6	-			31	CKB-
	CLK	CLK	CLK			32	CKB+

2



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

	Bit mapping	Transmitter Pin Assign		Output Connector		CN2	
		Single type LVDS Tx	Dual type LVDS Tx Thine THC63LVD1023B			Pin No.	Signal Name
odd Pixel data C	RC4	TA0	R14	CTA-	→	-	-
	RC5	TA1	R15			4	DC0-
	RC6	TA2	R16			5	DC0+
	RC7	TA3	R17			-	-
	RC8	TA4	R18	CTB-	→	7	DC1-
	RC9	TA5	R19			8	DC1+
	GC4	TA6	G14			-	-
	GC5	TB0	G15			-	-
	GC6	TB1	G16	CTC-	→	10	DC2-
	GC7	TB2	G17			11	DC2+
	GC8	TB3	G18			-	-
	GC9	TB4	G19			-	-
	BC4	TB5	B14	CTD-	→	16	DC3-
	BC5	TB6	B15			17	DC3+
	BC6	TC0	B16			-	-
	BC7	TC1	B17			-	-
	BC8	TC2	B18	CTE-	→	19	DC4-
	BC9	TC3	B19			20	DC4+
	Hsync	TC4	Hsync			-	-
	Vsync	TC5	Vsync			-	-
	DE	TC6	DE	CTCLK-CTCLK+	→	13	CKC-
	RC2	TD0	R12			14	CKC+
	RC3	TD1	R13			-	-
	GC2	TD2	G12			-	-
	GC3	TD3	G13	DTA-	→	23	DD0+
	BC2	TD4	B12			-	-
	BC3	TD5	B13			-	-
	N.C.	TD6	-			-	-
even Pixel data D	RC0	TE0	R10	DTB-	→	25	DD1-
	RC1	TE1	R11			26	DD1+
	GC0	TE2	G10			-	-
	GC1	TE3	G11			-	-
	BC0	TE4	B10	DTC-	→	28	DD2-
	BC1	TE5	B11			29	DD2+
	N.C.	TE6	-			-	-
	CLK	CLK	CLK			-	-
	RD4	TA0	R14	DTD-	→	34	DD3-
	RD5	TA1	R15			35	DD3+
	RD6	TA2	R16			-	-
	RD7	TA3	R17			-	-
	RD8	TA4	R18	DTE-	→	37	DD4-
	RD9	TA5	R19			38	DD4+
	GD4	TA6	G14			-	-
	GD5	TB0	G15			-	-
	GD6	TB1	G16	DTCLK-DTCLK+	→	31	CKD-
	GD7	TB2	G17			32	CKD+
	GD8	TB3	G18			-	-
	GD9	TB4	G19			-	-
	BD4	TB5	B14	DTE+	→	-	-
	BD5	TB6	B15			-	-
	BD6	TC0	B16			-	-
	BD7	TC1	B17			-	-
	BD8	TC2	B18	DTCLK-DTCLK+	→	-	-
	BD9	TC3	B19			-	-
	Hsync	TC4	Hsync			-	-
	Vsync	TC5	Vsync			-	-
	DE	TC6	DE	DTE-	→	-	-
	RD2	TD0	R12			-	-
	RD3	TD1	R13			-	-
	GD2	TD2	G12			-	-
	GD3	TD3	G13	DTE+	→	-	-
	BD2	TD4	B12			-	-
	BD3	TD5	B13			-	-
	N.C.	TD6	-			-	-
	RD0	TE0	R10	DTCLK-DTCLK+	→	-	-
	RD1	TE1	R11			-	-
	GD0	TE2	G10			-	-
	GD1	TE3	G11			-	-
	BD0	TE4	B10	DTCLK-DTCLK+	→	-	-
	BD1	TE5	B11			-	-
	N.C.	TE6	-			-	-
	CLK	CLK	CLK			-	-

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.8 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display 1,073,741,824 colors equivalent with 1,024 gray scale in each R, G, B sub-pixel.
Also the relation between display colors and input data signals is as follows.

Display colors		Data signal (0: Low level, 1: High level)																																																	
		RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	GD9	GD8	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	CG9	CG8	CG7	CG6	CG5	CG4	CG3	CG2	CG1	CG0	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	ED9	ED8	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0	FA9	FA8	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
		RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	GA9	GA8	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	HA9	HA8	HA7	HA6	HA5	HA4	HA3	HA2	HA1	HA0	IA9	IA8	IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	JA9	JA8	JA7	JA6	JA5	JA4	JA3	JA2	JA1	JA0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Cyan	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	↑																																																		
						:																																													
						:																																													
	↓	1	1	1	1	1	1	1	1	1	0	0																																							
	bright	1	1	1	1	1	1	1	1	1	0	1																																							
Red	1	1	1	1	1	1	1	1	1	1	0																																								
	1	1	1	1	1	1	1	1	1	1	1																																								
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	↑																																																		
						:																																													
						:																																													
	↓	0	0	0	0	0	0	0	0	0	0	0																																							

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.9 INPUT SIGNAL TIMINGS

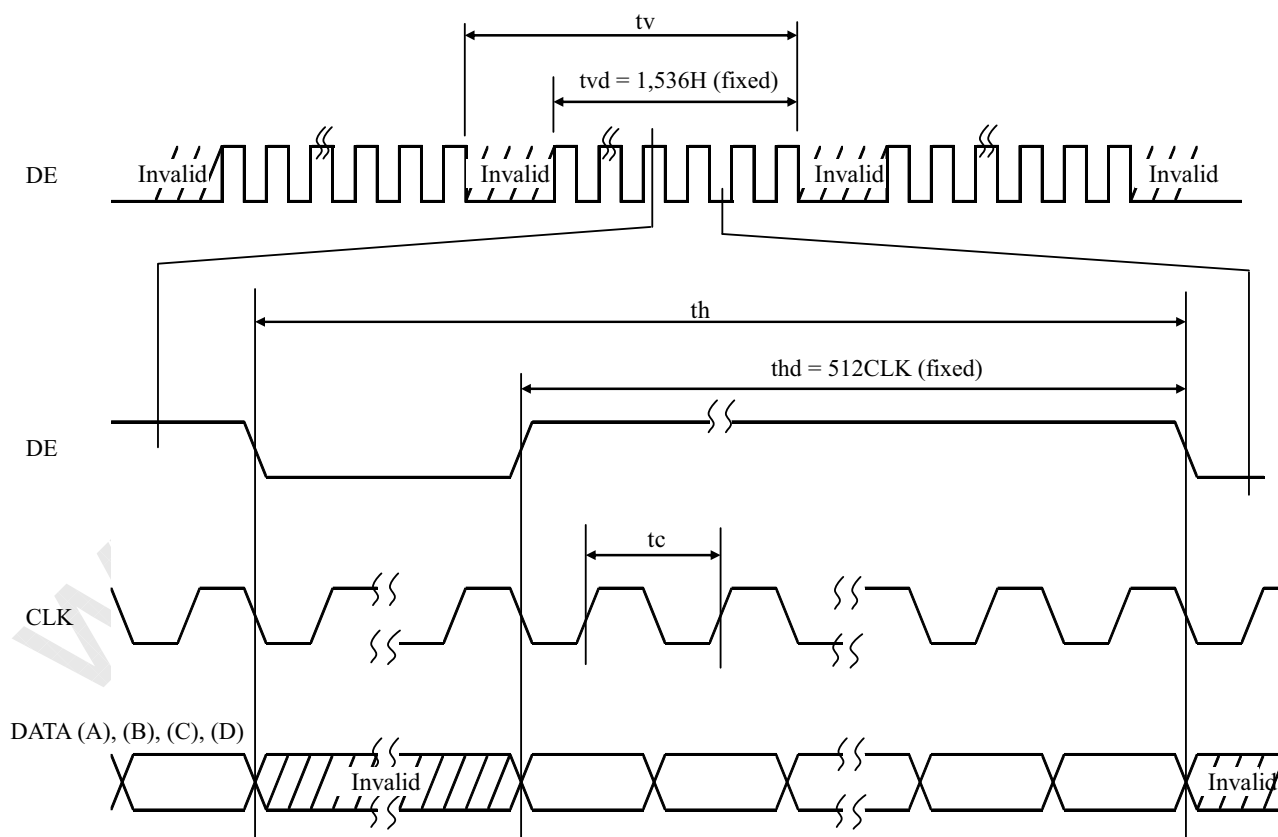
4.9.1 Timing characteristics

 $f_v=60\text{Hz}$

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/ tc	60.0	65.0	66.0	MHz	-
	Duty		-	See the data sheet of LVDS transmitter.			-	-
	Rise time, Fall time		-				ns	-
DE	Horizontal	Cycle	th	10.34	10.34	10.77	μs	96,72kHz(typ.)
				640	672	700	CLK	Note1
		Display period	thd	512			CLK	-
	Vertical	Cycle	tv	15.47	16.667	17.9	ms	60.0Hz(typ.)
				1547	1612	1628	H	
			Display period	tvd	1536			H
	CLK-DE	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
Rise time, Fall time		-	ns				-	

Note1: The sum of jitter and skew of horizontal period should be within ± 1 CLK.

4.9.2 Input signal timing chart

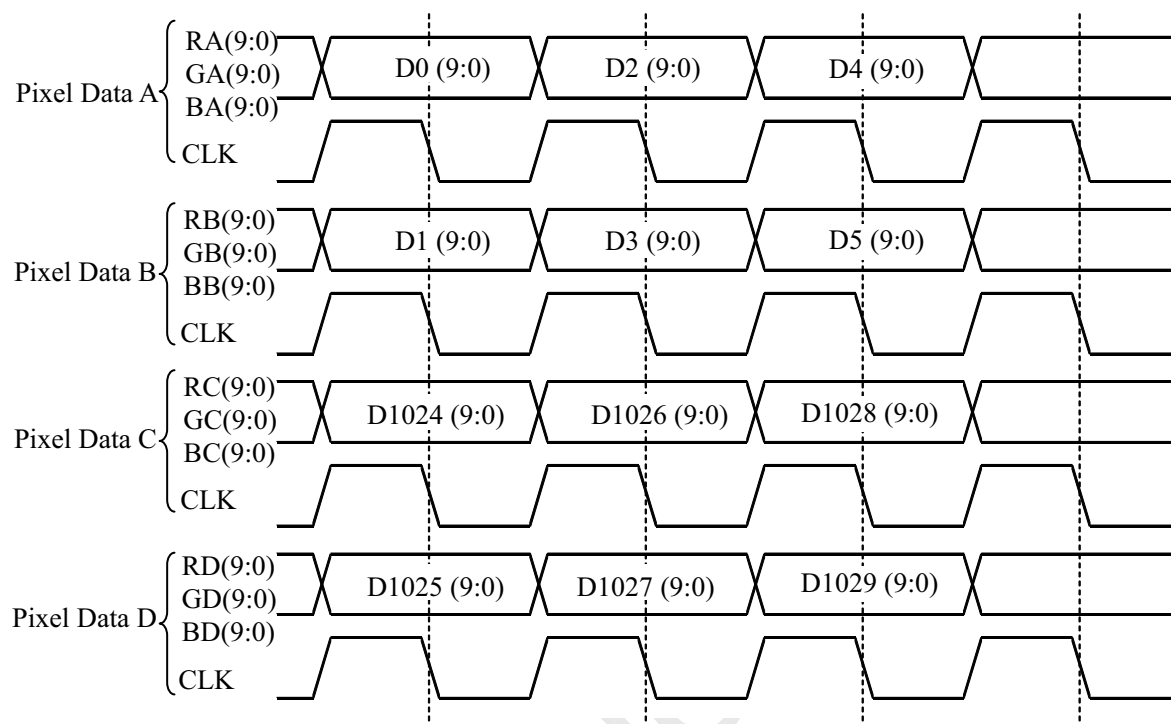


PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

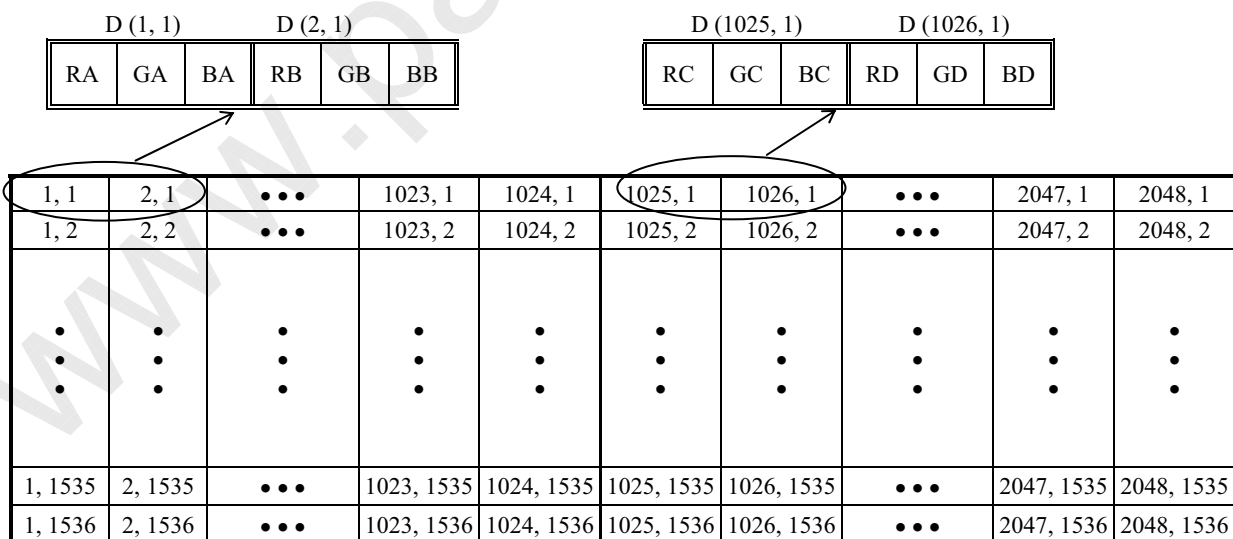
4.10 LVDS DATA TRANSMISSION METHOD



4.11 DISPLAY POSITIONS

Odd pixel: RA,RC= Red date
GA,GC=Green date
BA,BC=Blue date

Even pixel: RB,RD=Red date
GB,GD=Green date
BB,BD=Blue date

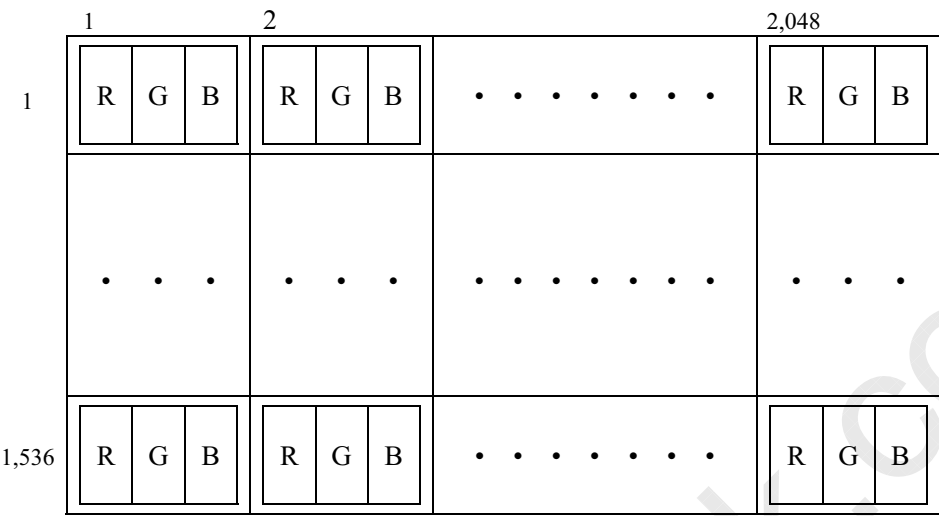


PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.12 PIXEL ARRANGNMENT



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

4.13 OPTICS

4.13.1 Optical characteristics

(Note1, Note2)

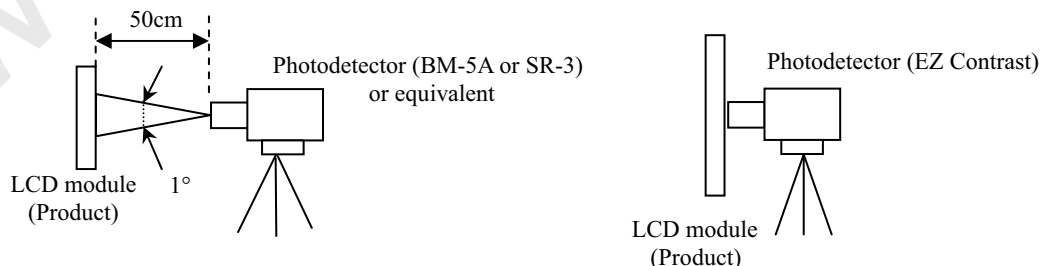
Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	L	TBD	800	-	cd/m ²	BM-5A or SR-3	Note3
Contrast ratio		White/Black at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	CR	TBD	1,400	-	-	BM-5A or SR-3	Note3 Note5
Luminance uniformity		1023/1023 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU1023	(80)	-	-	%	BM-5A or SR-3	Note4 Note6
Chromaticity	White	x coordinate	Wx	(0.269)	0.299			Note3 Note8	
		y coordinate	Wy	(0.285)	0.315	(0.345)	-		
	Red	x coordinate	Rx	-	(0.65)	-	-		
		y coordinate	Ry	-	(0.33)	-	-		
	Green	x coordinate	Gx	-	(0.29)	-	-		
		y coordinate	Gy	-	(0.60)	-	-		
	Blue	x coordinate	Bx	-	(0.15)	-	-		
		y coordinate	By	-	(0.07)	-	-		
Color uniformity		818/1023 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	Δu'v'	-	-	0.01	-	SR-3	Note4 Note7
Color gamut		θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	C	(65)	(72)	-	%	SR-3	Note3
Response time		Black to White	Ton	-	(20)	(30)	ms	BM-5A	Note3 Note9
		White to Black	Toff	-	(20)	(30)	ms		
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	70	88	-	°	BM-5A or EZ Contrast	Note3 Note10
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	70	88	-	°		
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	70	88	-	°		
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	70	88	-	°		

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta= 25°C, VDD= 12.0V, VDDb= 12.0V, PWM: Duty 100%, Display mode: QXGA,
Horizontal cycle= 1/96.72 kHz, Vertical cycle= 1/60.0 Hz

Optical characteristics are measured at luminance saturation 20minutes after the product works in the dark room. Also measurement methods are as follows.



Note3: Product surface temperature at the maximum luminance control: TopF = 32°C

Note4: Product surface temperature at 450cd/m² luminance control: TopF = 30°CTemperature difference in display area: $\Delta T_{BD}^\circ C$

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

Note5: See "4.13.2 Definition of contrast ratio".

Note6: See "4.13.3 Definition of luminance uniformity".

Note7: See "4.13.4 Definition of color uniformity".

Note8: These coordinates are found on CIE 1931 chromaticity diagram.

Note9: See "4.13.5 Definition of response times".

Note10: See "4.13.6 Definition of viewing angles".

2

4.13.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

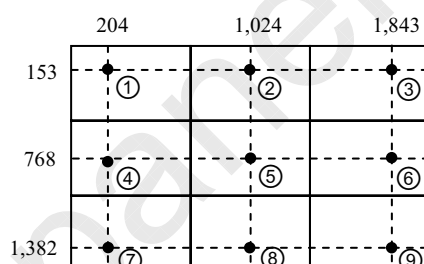
4.13.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity (LU}_{xx}) = \frac{\text{Minimum luminance from ① to ⑨}}{\text{Maximum luminance from ① to ⑨}}$$

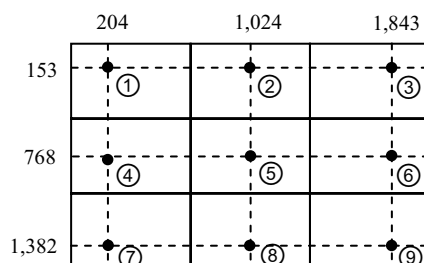
xx: 0, 104, 512, 816, 1023 gray scale.

The luminance is measured at near the 9 points shown below.



4.13.4 Definition of color uniformity

The color (u' , v') is measured at near the 9 points shown below.



2

The color uniformity in each measuring point is calculated by using the following formula.

$$\text{Color uniformity}(\Delta u'v') = \sqrt{(u'_x - u'_y)^2 + (v'_x - v'_y)^2}$$

u'_x, v'_x : u' , v' value at measuring point x.

u'_y, v'_y : u' , v' value at measuring point y.

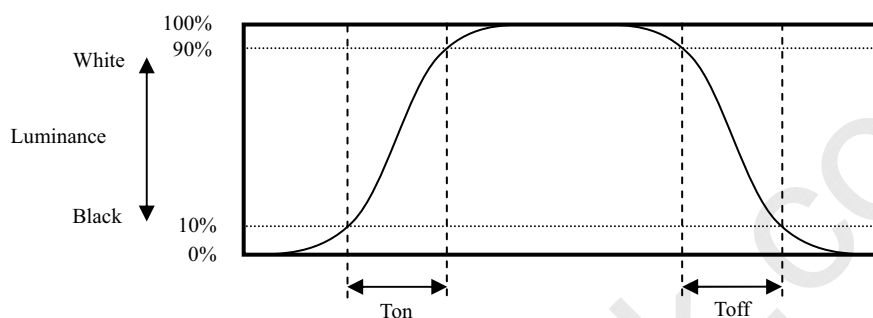
PRELIMINARY

NLT Technologies, Ltd.

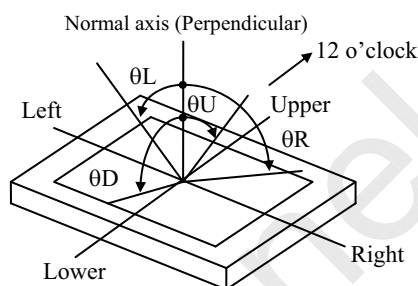
NL204153AC21-17

4.13.5 Definition of response times

Response time is measured at the time when the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time when the luminance changes from 10% up to 90%. Also Toff is the time when the luminance changes from 90% down to 10% (See the following diagram.).



4.13.6 Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM: Duty 100%	70,000	h
	60°C (Surface temperature at screen) Continuous operation, PWM: Duty 100%	TBD	

Note1: Life time expectancy is mean time to half-luminance.

Note2: Estimated luminance lifetime is not the value for an LCD module but the value for LED elementary substance.

Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

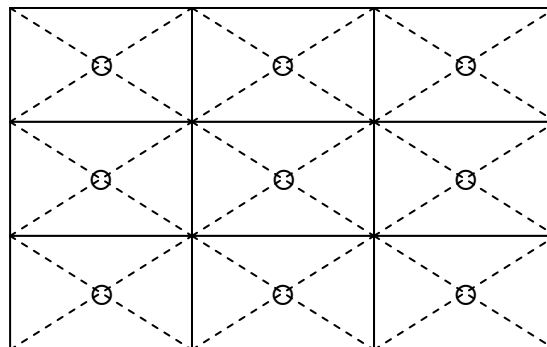
6. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① $60 \pm 2^{\circ}\text{C}$, RH= 60%, 500hours ② Display data is white. Note2	No display malfunctions
Heat cycle (Operation)		① $0 \pm 3^{\circ}\text{C}$...1hour $60 \pm 3^{\circ}\text{C}$...1hour ② 50cycles, 4hours/cycle ③ Display data is white. Note2	
Thermal shock (Non operation)		① $-20 \pm 3^{\circ}\text{C}$...30minutes $60 \pm 3^{\circ}\text{C}$...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s^2 , 11ms ② X, Y, Z directions ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, $\pm 10\text{kV}$ ② 9 places on a panel surface Note3 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval Note2	
Low pressure	Non-operation	① 15kPa (Equivalent to altitude 13,600m) ② $-20^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours ③ $+60^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours	No display malfunctions
	Operation	① 53.3kPa (Equivalent to altitude 4,850m) ② $0^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours ③ $+60^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours Note2	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: Luminance: 450cd/m^2 at luminance control.

Note3: See the following figure for discharge points





PRELIMINARY

NLT Technologies, Ltd.**NL204153AC21-17**

7. PRECAUTIONS

7.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "7.2 CAUTIONS" and "7.3 ATTENTIONS"!**



This sign has the meaning that a customer will be injured or the product will sustain damage if the customer practices wrong operations.



This sign has the meaning that a customer will be injured if the customer practices wrong operations.

7.2 CAUTIONS



*** Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: Equal to or no greater than 294m/s^2 and equal to or no greater than 11ms, Pressure: Equal to or no greater than 19.6N ($\phi 16\text{mm}$ jig))**

7.3 ATTENTIONS



7.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed 0.735N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be $\leq 5.0\text{mm}$.

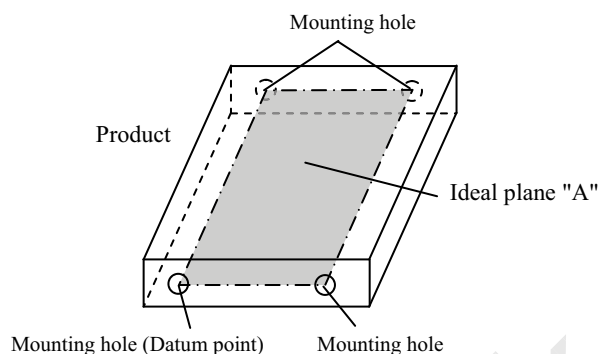
PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.

Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ± 0.3 mm.



- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, wipe it with a soft dry cloth.
- ⑧ Do not push or pull the interface connectors while the product is working.
- ⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
- ⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

7.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
- ③ Do not operate in high magnetic field. If not, circuit boards may be broken.
- ④ This product is not designed as radiation hardened.



PRELIMINARY

NLT Technologies, Ltd.**NL204153AC21-17**

7.3.3 Characteristics

The following items are neither defects nor failures.

- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
- ③ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen. 2
- ④ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑤ Optical characteristics may be changed depending on input signal timings.

7.3.4 Others

- ① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ Pack the product with the original shipping package, in order to avoid any damages during transportation, when returning the product to NLT for repairing and so on.
- ④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

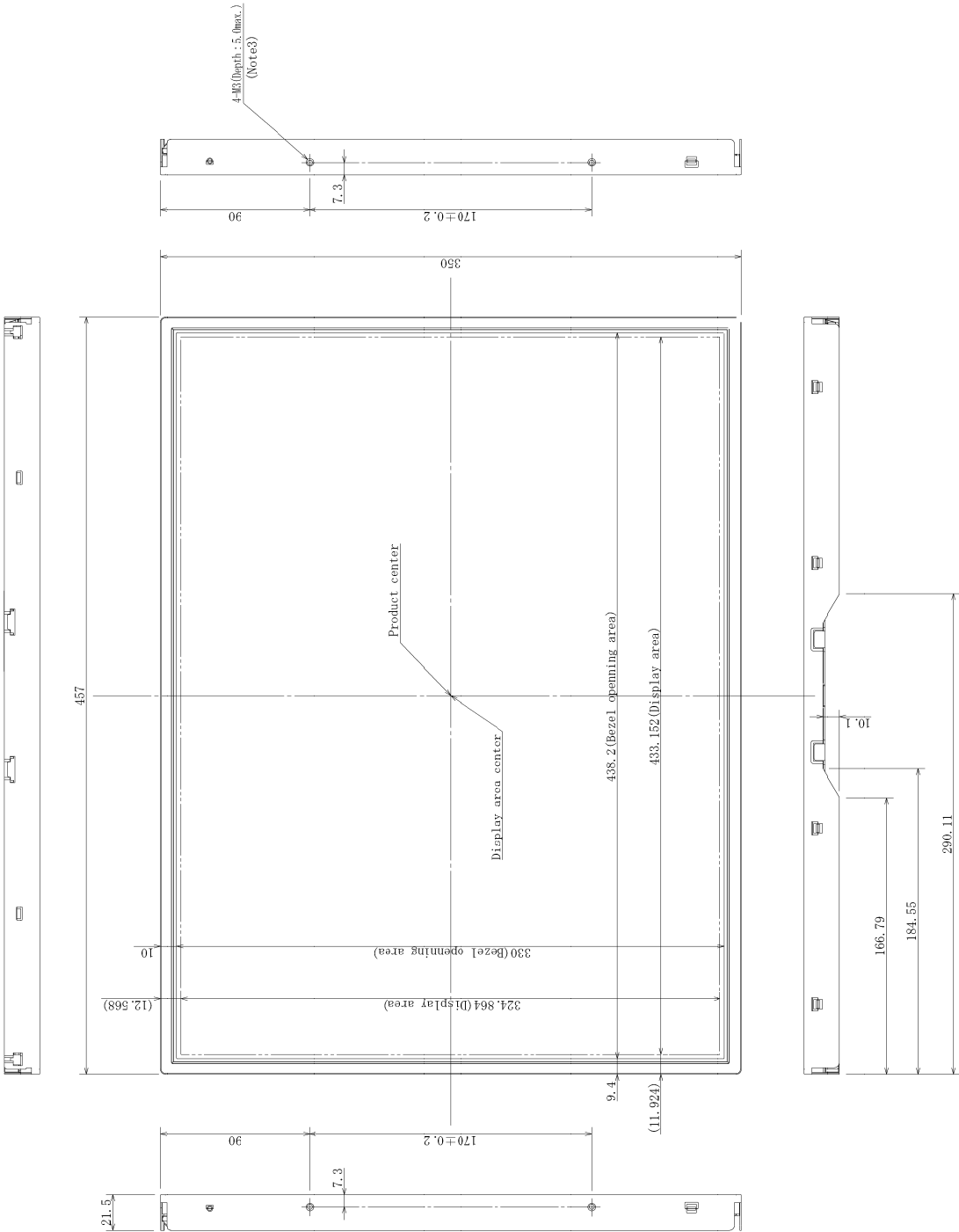
PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

8. OUTLINE DRAWINGS

8.1 FRONT VIEW



- Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

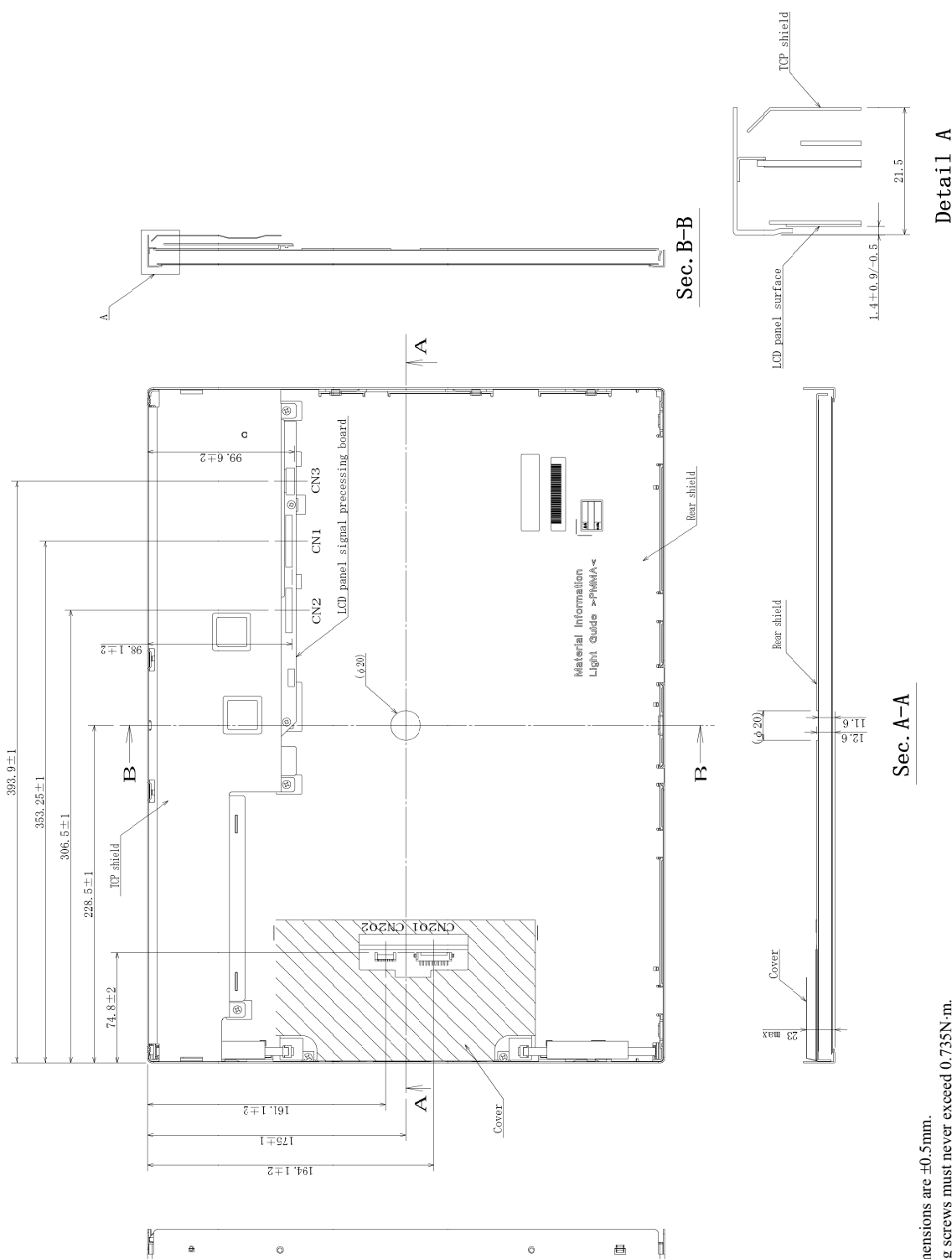
Unit: mm

PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

8.2 REAR VIEW



Unit: mm

Note1: Not shown tolerances of the dimensions are $\pm 0.5\text{mm}$.
 Note2: The torque for product mounting screws must never exceed $0.735\text{N}\cdot\text{m}$.
 Note3: The length of product mounting screws from surface of plate must be $\leq 5.0\text{mm}$.
 Note4: The values in parentheses are for reference.



PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-1243	July 8, 2011	Revision contents New issue Writer <i>Approved by</i> T. OGAWA <i>Checked by</i> _____ <i>Prepared by</i> T. OGAWA
2nd edition	DOD-PP-1266	Sep 16, 2011	Revision contents P5 General specifications • Luminance: 770 cd/m² (typ.) → 800 cd/m² (typ.) • Signal system: THC63LVD824 → THC63LVD104S • Power consumption: (54) W (typ.) → (58) W (typ.) P7 Mechanical specifications • Module size: TBD (max. D) mm → 23.0 (max. D) mm • Weight: TBD (max.) g → (2,980) (max.) g P7 Absolute maximum ratings • Power supply voltage- LED driver board: -0.3 to +27.0 V → -0.3 to +15.0 V • Operating temperature- Rear surface: (0 to + TBD) °C → (0 to + 60) °C P8 LCD panel signal processing board • Power supply current: (700) (typ.), TBD (max.) mA → (590) (typ.), (980) (max.) mA P9 LED Driver board • Power supply current: (5,000) (typ.) mA → (4,200) (typ.) mA P9 LED Driver board current wave • (5,000) mA (typ.) → (4,200) mA (typ.) • At the minimum luminance control: TBD % → (1) % (At frequency: 325 Hz) P10 Power supply voltage ripple (addition), Fuse (addition) P11 LED Driver board • tr ≤ TBD ms → tr ≤ (100) ms • Note2: TBD → (100) ms P17 Luminance control methods • Variable resistor control- Luminance ratio: 0Ω: TBD % → 0 % • Voltage control- Luminance ratio: 0V: TBD % → 0 % • Pulse width modulation- Luminance ratio : TBD, TBD % → (0.01), (1) %, (At frequency: 325 Hz) P18 Detail of BRTP timing- Each parameter • Luminance control frequency: (325) (max.) Hz → (1,000) (max.) Hz • Parameter: Duty ratio → External PWM pulse width P19-20 Method of connection for LVDS transmitter • Transmitter: THC63LVD104S → THC63LVD1023B P25-26 Optical characteristics • Luminance: 770 cd/m² (typ.) → 800 cd/m² (typ.) • Color uniformity (addition) • Response time: Ton / Toff: TBD (max.) ms → (30) (max.) ms • Viewing angle- Measuring instrument: BM-5A (addition) • Note3: TopF = TBD°C → TopF = 32°C • Note4: TopF = TBD°C → TopF = 30°C • Temperature difference in display area: ΔTBD°C (addition) • Note7 (addition) • Definition of color uniformity (addition)

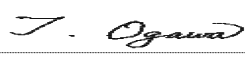
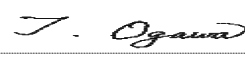
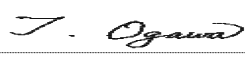
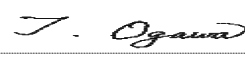
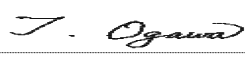
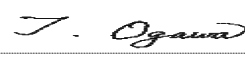


PRELIMINARY

NLT Technologies, Ltd.

NL204153AC21-17

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature									
2nd edition	DOD-PP-1266	Sep 16, 2011	Revision contents P31 Characteristics • Optical characteristics ..., because the LCD has cold cathode fluorescent lamps. (elimination) P32-33 Outline drawings- Front view • Front view • 7.5 → 7.3 (2 points), 8.9 → 10.1 • Display center → Product center • 92, 122.3 (elimination) • 166.79, 184.55, 290.11 (additon) • Rear view • Cover: figure is changed. Signature of writer <table><tr><td>Approved by</td><td>Checked by</td><td>Prepared by</td></tr><tr><td></td><td></td><td></td></tr><tr><td>T. OGAWA</td><td></td><td>T. OGAWA</td></tr></table>	Approved by	Checked by	Prepared by				T. OGAWA		T. OGAWA
Approved by	Checked by	Prepared by										
												
T. OGAWA		T. OGAWA										